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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,981	05/02/2001	Jason Seung-Min Kim	2100653-991340	5778

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EXAMINER	
SCHNEIDER, JOSHUA D	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,981	KIM, JASON SEUNG-MIN	
	Examiner	Art Unit	
	Joshua D. Schneider	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/16/2005 have been fully considered but they are not persuasive. However new rejections are set forth below in light of the arguments.

2. With regards to the rejection under 35 U.S.C. 112, second paragraph, applicant has again argued that a software DMA system cannot be taught by references that require the use of hardware, and it is again unclear that to what level of software is required. Software is well known to be running in the operation of almost any processor in the form of microprograms, as is taught by Tanenbaum. Tanenbaum teaches that such simple operations such as counting and clocking may be handled by such microprograms. It is unclear, based of Applicant's admission that a hardware processor is in fact necessary, to what extent the applicant is basing the software DMA engine in software and what is in hardware.

3. With regards to the rejections under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,884,027 to Garbus et al. in further view of "Structured Computer Organization" by Tanenbaum, applicant begins with the argument that not all of the limitations are taught by Garbus. This statement is true, but is irrelevant as the rejection is an obvious rejection. Applicant has also argued that the combination and arrangement of the components in Garbus are significantly different than those that are claimed. Applicant fails to point to what these differences are, or to how the rejections as stated are incorrectly mapped to the limitations of the claims, so this argument holds no weight. Applicant seems to argue with regards to claim 6 that the PCI to PCI bridge processor is not processor.

4. Applicant has not specifically pointed out what is lacking in the rejection. Applicant has argued that Garbus does not teach a first processor coupled to a first bus or a second processor coupled to a second bus. This argument does not have any evidentiary support and seems to be entirely fallacious given the presented evidence in the previous rejections.

5. Applicant has also argued that Garbus does not teach a software DMA engine that is executed by the one of the first and second processors. While this argument is true, it is wholly ineffective to overcome the rejection, as the rejections make clear that the examiner has never made such an assertion. It is the teachings of the other references that make it clear that one of ordinary skill in the art at the time of invention would have known that hardware and software are logically equivalent, and therefore interchangeable as a matter of design.

6. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

7. Applicant has further argued of the first paragraph of page 3 that the characterization of Garbus' system 31 as teaching the second processor of claim 1 is factually incorrect because it conflicts with the explicit description in Garbus. Again this assertion by the Applicant has no evidentiary support. The mere fact that other elements are integrated in to the same device to form a single system does not eliminate the presence of a processor as clearly shown by the drawings in Garbus.

8. Applicant then argues that Garbus' teaching DMA controllers' 51a and 51b that refute Examiner's assignment of DMA functionality to system 31. This allegation is again unclear, as

the DMA controllers are part of the system that the processor controls. Applicant then states that the two DMA controllers 51a and 51b operate independently of local processor 34 to transfer data. This is yet another argument that is not supported by the evidence. Garbus clearly and explicitly teaches that the local processor 34 is used to program the DMA controllers (column 3, lines 41-46).

9. The next argument is that Garbus does not teach local processor 34 coupled to a first bus and a second bus such that it could execute a DMA engine capable of transferring data directly between all of a plurality of resources connected to at least one of the first bus and the second bus, and that the specific processor taught in the preferred Garbus embodiment has a single address/data bus and is thus incapable of being coupled to more than one bus. This argument is again not supported by the evidence, though it is most likely due to the interpretation of the claim language being made by the Applicant. The word coupled here appears to be confused by the Applicant with the word connected. While it may be true that the second processor is not connected to both the first and second bus, it is certainly at least coupled, thought the DMA controllers or otherwise. The existence of other devices connected between the processor and the two busses does not eliminate a coupling, but only a direct connection.

10. Furthermore, the specific preferred embodiment of Garbus cannot be said eliminate the teaching or suggestion a processor capable of executing a DMA engine. The specific embodiment of Garbus is not being relied upon, but rather the larger teachings of Garbus. These teachings are further being altered in the rejection by the use of secondary references. The broader teachings of Garbus are what are being relied upon. The rejection never makes any reference to requiring the use of a functionally unmodified Intel 80960 JF processor, nor is the

use of one required by Garbus. The very fact that the use of such a processor is described in the *preferred embodiment* of the invention should make clear that this is not the only embodiment that can be found from the teachings of Garbus, but rather a preferred specific implementation.

11. The next argument is that Garbus does not teach the instruction memory for storing the software DMA engine. This is again not asserted by the rejection, but is obvious in light of the other references provided. One of ordinary skill in the art at the time of invention would have known that hardware and software are logically interchangeable as taught by Tanenbaum. In Garbus, the DMA transfers are effectuated by the processor programming the DMA controllers, (column 3, lines 38-46). These DMA controllers are hardware devices. If one were to change these hardware devices into software that effectuated the same operations, one would have to turn the hardware logic into the bits of code that would make up the software. In making such a transformation, one of ordinary skill in the art would realize that the software cannot simply exist in the ether, but must be stored in some sort of memory that the processor can access in order to effectuate the same DMA transfer that it was doing in hardware. Therefore, the use of instruction memory is logically inherent to the implementation of DMA in software.

12. Applicant argues that the Tanenbaum does not teach how an Intel 80960 JF processor can be coupled to the first and second busses. It is again pointed out that the rejection in no way relies upon the use of an Intel 80960 JF processor.

13. Applicant has argued that the Boyle reference does cure the problem of teaching all the claim limitations. Again, it should be clear from the fact that this is a rejection under 35 U.S.C. 103(a), and not under 35 U.S.C. 102, that all of the limitations are not going to be taught by any one reference. Rather it is the combination of the teaching of the multiple references that is

pertinent. The new rejection as set forth below to clarify the rejection in preparation for appeal if necessary.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

16. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "software direct memory access" in claims 1-5 is used by the claim to mean "software based direct data transfer by a processor", while the accepted meaning is "software based direct data transfer without the use of the processor." The term is indefinite because the specification does not clearly redefine the term.

17. A DMA transfer by definition a transfer that does not involve the processor for the transfer operations. The purpose of these types of transfers is to offload the task of transferring data from the processor(s). It is unclear what level of software involvement is required to execute the DMA transfer, and whether the software is a microprogram or an application. This makes it unclear as to whether any microprograms running on the processor may be considered

to be a "software DMA engine," as such microprograms are coupled to the processor that is coupled to the busses.

18. Applicant has again set forth that the DMA engine of the instant invention requires no hardware to operate. It is well known in that art that software cannot function without the use of hardware. At no point in the specification is it found where the DMA software engine can operate without hardware support. In fact, the claims require the use of a processor, and it is well known in the art that processors usually have other hardware devices associated with them in order to operate. Applicant is therefore invited to point to any parts of the specification that teach that the invention can be practiced without any hardware.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,884,027 to Garbus et al. in further view of "Structured Computer Organization" by Tanenbaum and U.S. Patent 6,668,287 to Boyle.

21. With regards to claim 1, Garbus teaches a first processor coupled to a first bus (Figs. 2, elements 25 and 17), a second processor coupled to a second bus (Figs. 2, elements 31 and 19), and a DMA engine in the second processor capable of executing the transfer of data between system resources connected to at least one of the first bus and the second bus (column 2, lines 9-33). Garbus does not explicitly teach the DMA engine is a software engine. In fact Garbus

refers to the use of hardware, including DMA registers and a DMA controller in the P2P processor. However, it is well known that not all devices are hardware DMA compatible, and must be accessed using software DMA. Tanenbaum also teaches that hardware and software are logically interchangeable (page 11, third paragraph). Boyle teaches that DMA hardware implementations are complicated and costly (column 2, lines 2-28). To eliminate this cost, it is logical to turn to software that is logically interchangeable and taught by Tanenbaum. Such a software implementation is taught by Boyle (column 6, lines 3-67). It would have been obvious to one of ordinary skill in the art at the time of invention to replace the hardware DMA controller with a software DMA engine in order to eliminate the cost and space needed to implement hardware DMA.

22. With regards to claims 5 and 6, Garbus teaches the loading of multiple data packets from a device and storing these multiple data packets into the system memory at the specified locations (scatter/gather data chaining, column 42, line 44, through column 43, line 33).

23. With regards to claims 2 and 9, Garbus teaches the processing of data (scatter/gather and unaligned data transfer, column 42, line 44, through column 43, line 33).

24. With regards to claims 3 and 7, Garbus teaches RAM memories (column 3, lines 29-45) and hardware buffers for interfacing with devices (column 42, line 44, through column 43, line 33).

25. With regards to claims 4 and 8, Garbus teaches DMA through the use of hardware buffers for interfacing with devices (column 42, line 44, through column 43, line 33).

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D. Schneider whose telephone number is (571) 272-4158. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIM HUYNH
PRIMARY EXAMINER
12/22/05